

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Gilbert Wolrich et al.      Art Unit: 2183  
Serial No.: 09/760,509      Examiner: Aimee J. Li  
Filed: January 12, 2001      Conf. No.: 2157  
Title: METHOD AND APPARATUS FOR PROVIDING LARGE REGISTER  
ADDRESS SPACE WHILE MAXIMIZING CYCLETIME PERFORMANCE  
FOR A MULTI-THREADED REGISTER FILE SET

**Mail Stop Appeal**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Claims 1-7, 15-26, and 30-35 are pending. Independent claims 1, 15, and 19 all stand rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady") and U.S. Patent No. 5,787,454 to Rohlman (hereinafter "Rohlman"). Claims 1, 15, and 19 all relate to register sets that comprise a plurality of two-ported random access memory devices.

Claim 1, which is illustrative, recites that a register set comprises "a plurality of two-ported random access memory devices assembled into banks, the register set comprising two effective read ports and one effective write port, wherein the effective write port comprises write ports of a pair of the two-ported random access memory devices, each bank being capable of performing a read and a write to two different words in the same processor cycle."

The rejections of claims 1, 15, 19, and their dependencies are based on the contention that:

"Parady was relied upon to teach '... the register set comprising a plurality of two-ported random access memory devices assembled into banks (Parady 48 of Fig.1/Fig.3), each bank being capable of performing a

read and a write to two different words with two ports in the same processor cycle..." See, e.g., *Office action mailed March 13, 2008*, page 13, para. 38. See also *id.*, page 3, para. 7, c.

In particular, the rejection contends that:

"Parady shows in Figure 1, element 48 a register file with 10 ports and Parady teaches in column 3, lines 43-49 that the register file is split into 4 banks. This means that each bank has at least 2 ports, thereby allowing each bank to write or read at least 1 word per bank per cycle." See *Advisory action mailed June 19, 2008*, Continuation sheet.

Applicant respectfully disagrees and submits that, in light of the common erroneous reliance in the rejections of claims 1, 15, and 19 on a single excerpt of Parady, these rejections are appropriate for the abbreviated review provided by this program.

For the sake of convenience, the cited excerpt of Parady is now reproduced, along with excerpts from FIGS. 1, 3 that show integer register file 48.

"Integer register file 48 is divided up into four register files to support threads 0-3. ... This can be accomplished either by providing physically separate groups of registers for each thread, or alternately by providing separate register windows for each thread." See *Parady*, col. 3, lines 43-49.

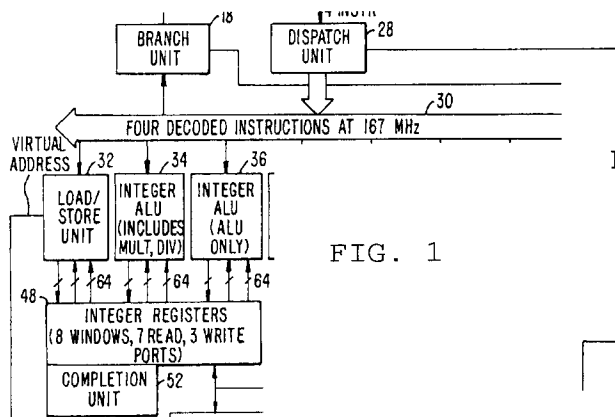


FIG. 1

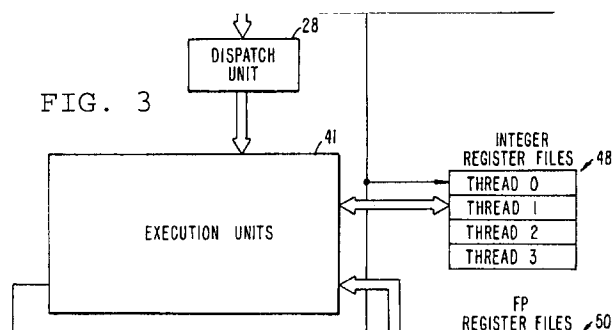


FIG. 3

In FIG. 3, instruction units 41 include the "multiple pipelines 32-46." See, e.g., *Parady*, col. 3, line 40-44. Thus, the selected excerpts of FIGS. 1 and 3 both show information flowing from dispatch unit 28, into execution units 41 (including pipelines 32, 34, 36), and into and out of register file 48.

As shown in FIG. 1, there are one write and two read ports between register file 48 and Load/Store unit 32. There are one write and two read ports between register file 48 and Integer ALU 34. There are one write and two read ports between register file 48 and Integer ALU 36.

As shown above, the rejection contends that the division of register file 48 into four register files by "by providing physically separate groups of registers for each thread, or alternately by providing separate register windows for each thread," inherently requires that register file 48 comprise "a plurality of two-ported random access memory devices assembled into banks, the register set comprising two effective read ports and one effective write port, wherein the effective write port comprises write ports of a pair of the two-ported random access memory devices, each bank being capable of performing a read and a write to two different words in the same processor cycle."

Applicant respectfully disagrees for several reasons. For example, the fact that "register file 48 is divided up into four register files" does not mean that these subdivision register files is somehow a "plurality of two-ported random access memory devices assembled into banks." Instead, each pipeline 32, 34, 36 is understood to require the same access to each of the subdivisions of register file 48 that is available between those pipelines and the undivided register file 48. In other words, the mere fact that register file 48 is divided up into four

register files to support threads 0-3 does not mean that any of Load/Store unit 32, Integer ALU 34, and Integer ALU 36 lose read and write access to any of the individual subdivisions.

Please note that this interpretation is fully consistent with Parady's indication that register file 48 can be divided "by providing physically separate groups of registers for each thread." To the extent that such a provision of separate groups of registers involves additional registers, it would appear that the read/write access to the duplicated registers by Load/Store unit 32, Integer ALU 34, and Integer ALU 36 is to remain unchanged. In other words, there are to be one write and two read ports between each subdivision of register file 48 and each of Load/Store unit 32, Integer ALU 34, and Integer ALU 36.

As contended throughout prosecution, there is no reason to believe that Parady's integer registers 48 constitute a register set that comprises a plurality of two-ported random access memory devices assembled into banks. Paraday is silent as to the architecture of integer registers 48. Instead, integer registers 48 appear to be standard registers with hardware ports as shown in FIG. 1.

In the absence of any grounds for believing that Parady's integer registers 48 comprise a plurality of two-ported random access memory devices assembled into banks, Applicant reiterates and incorporates by reference the Remarks regarding Rohlman set forth in the Responses filed December 11, 2007 and May 5, 2008. In particular, there is nothing in Rohlman that describes or suggests how to assemble Rohlman's cells into the recited banks.

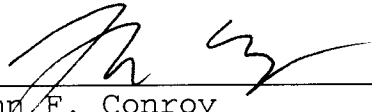
Applicant: Gilbert Wolrich et al. Attorney's Docket No.: 10559-317001 / P9678  
Serial No.: 09/760,509  
Filed: January 12, 2001  
Page: 5 of 5

Even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the subject matter recited in claims 1, 15, and 19. Claims 1, 15, and 19 are thus not obvious over Paraday and Rohlman and Applicant respectfully requests that the rejections of these claims and the claims dependent therefrom be withdrawn.

All rights to address additional matters on appeal in any subsequent appeal brief are reserved. Please apply the Notice of Appeal fee, along with any other charges or credits, to deposit account 06-1050.

Respectfully submitted,

Date: July 14, 2008

  
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